

# Claims

- [c1] 1. A wafer bumping process, comprising the steps of:  
providing a wafer, said wafer comprising a plurality of bonding pads and a passivation layer covering a surface of said wafer and exposing said bonding pads;  
forming a first under bump metallurgy layer covering said passivation layer and said bonding pads;  
forming a first patterned photoresist layer on said first under bump metallurgy layer, said first patterned photoresist layer comprising a plurality of first openings corresponding to said bonding pads and exposing a portion of said first under bump metallurgy layer;  
forming a second under bump metallurgy layer within said first openings;  
forming a second patterned photoresist layer on said first patterned photoresist layer, said second patterned photoresist layer comprising a plurality of second openings, said second openings being larger than said first openings to expose a portion of said second under bump metallurgy layer;  
filling said second openings with a solder material, wherein the solder material covers said exposed portion of said second under bump metallurgy layer;

reflowing said solder material to form a plurality of solder bumps;  
removing said second patterned photoresist layer and said first patterned photoresist layer to expose a portion of said first under bump metallurgy layer; and  
removing said exposed portion of said first under bump metallurgy layer.

[c2] 2. The wafer bumping process of claim 1, wherein the step of filling said solder material includes printing.

[c3] 3. The wafer bumping process of claim 1, wherein the step of filling said solder material includes electroplating.

[c4] 4. The wafer bumping process of claim 1, wherein side-walls of said second openings are slanting and said second openings expose said portion of said second under bump metallurgy layer.

[c5] 5. The wafer bumping process of claim 4, wherein said second openings taper towards said second under bump metallurgy layer within said first openings to expose said portion of said second under bump metallurgy layer.

[c6] 6. The wafer bumping process of claim 1, wherein said the step of forming first under bump metallurgy

layer includes sputtering deposition.

- [c7] 7. The wafer bumping process of claim 1, wherein the step of forming second under bump metallurgy layer includes electroplating.
- [c8] 8. The wafer bumping process of claim 1, wherein a material of said first under bump metallurgy layer is selected from the group of materials consisting of Cr, Ti, Ti-W alloy, Cu, Ni, Cr-Cu alloy, Ni-V alloy, Ni-Au alloy, and Al.
- [c9] 9. The wafer bumping process of claim 1, wherein a thickness of the said second under bump metallurgy layer is about 30–75 $\mu$ m.
- [c10] 10. The wafer bumping process of claim 1, wherein a material of said second under bump metallurgy layer having a melting point larger than a melting point of said solder material.
- [c11] 11. The wafer bumping process of claim 10, wherein a material of said second under bump metallurgy layer includes Cu.
- [c12] 12. The wafer bumping process of claim 10, wherein a material of said second under bump metallurgy layer includes Ni.

- [c13] 13. The wafer bumping process of claim 1, wherein a material of said solder material includes a Sn-Pb alloy.
- [c14] 14. The wafer bumping process of claim 1, wherein a material of said solder material includes a Sn-Ag-Cu alloy.
- [c15] 15. The wafer bumping process of claim 1, wherein a material of said solder material includes a high lead solder.
- [c16] 16. A structure of bumps comprising:  
a substrate having at least an active surface;  
a plurality of bonding pads formed on the active surface;  
a passivation layer formed over the active surface of the substrate, wherein portions of the bonding pads are exposed by the passivation layer;  
a first under bump metallurgy layer formed on the exposed portions of the bonding pads;  
a second under bump metallurgy layer formed on the first under bump metallurgy layer and  
a plurality of solder bumps formed on the second under bump metallurgy layer, wherein a melting point of the solder bumps is lower than a melting point of the second under bump metallurgy layer.
- [c17] 17. The structure of claim 16, wherein a material of the

second under bump metallurgy layer includes Cu.

- [c18] 18. The structure of claim 16, wherein the second under bump metallurgy layer is a nickel layer.
- [c19] 19. The structure of claim 16, wherein a thickness of the second under bump metallurgy layer is larger than that of the first under bump metallurgy layer.
- [c20] 20. The structure of claim 16, wherein a thickness of the second under bump metallurgy is about 30–75 $\mu\text{m}$ .
- [c21] 21. The structure of claim 16, wherein the first under bump metallurgy is composed of Ti, Ni–V alloy and Cu and directly formed on the exposed portions of the bonding pads.